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Area, Delay and Power Comparison of Adder Topologies

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ABSTRACT

Adders form an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area.This paper presents the pertinent choice for selecting the adder topology with the tradeoff between delay, power consumption and area. The adder topology used in this work are ripple carry adder, carry look ahead adder, carry skip adder, carry select adder, carry increment adder, carry save adder and carry bypass adder. The module functionality and performance issues like area, power dissipation and propagation delay are analyzed at 0.12µm 6metal layer CMOS technology using microwind tool.

KEYWORDS

Ripple Carry Adder, Carry Save Adder, Carry Increment Adder, Carry Select Adder.

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Low Power Reversible Parallel Binary Adder/Subtractor

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ABSTRACT

In recent years, Reversible Logic is becoming more and more prominent technology having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. Reversibility plays an important role when energy efficient computations are considered. In this paper, Reversible eight-bit Parallel Binary Adder/Subtractor with Design I, Design II and Design III are proposed. In all the three design approaches, the full Adder and Subtractors are realized in a single unit as compared to only full Subtractor in the existing design. The performance analysis is verified using number reversible gates, Garbage input/outputs and Quantum Cost. It is observed that Reversible eight-bit Parallel Binary Adder/Subtractor with Design III is efficient compared to Design I, Design II and existing design.

KEYWORDS

Reversible Logic, Garbage Input/output, Quantum Cost, Low Power, Reversible Parallel Binary Adder/Subtractor.

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An Efficient FPGA Implemenation of MRI Image Filtering and Tumour Characterization Using XILINX System Generator

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ABSTRACT

This paper presents an efficient architecture for various image filtering algorithms and tumor characterization using Xilinx System Generator (XSG). This architecture offers an alternative through a graphical user interface that combines MATLAB, Simulink and XSG and explores important aspects concerned to hardware implementation. Performance of this architecture implemented in SPARTAN-3E Starter kit (XC3S500E-FG320) exceeds those of similar or greater resources architectures. The proposed architecture reduces the resources available on target device by 50%.

KEYWORDS

MRI, Matlab, Xilinx System Generator, FPGA, Edge Detection.

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Comparative Performance Analysis of XORXNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design

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ABSTRACT

This paper presents comparative study of high-speed, low-power and low voltage full adder circuits. Our approach is based on XOR-XNOR design full adder circuits in a single unit. A low power and high performance 9T full adder cell using a design style called "XOR (3T)" is discussed. The designed circuit commands a high degree of regularity and symmetric higher density than the conventional CMOS design style as well as it lowers power consumption by using XOR (3T) logic circuits. Gate Diffusion Input (GDI) technique of low-power digital combinatorial circuit design is also described. This technique helps in reducing the power consumption and the area of digital circuits while maintaining low complexity of logic design. This paper analyses, evaluates and compares the performance of various adder circuits. Several simulations conducted using different voltage supplies, load capacitors and temperature variation demonstrate the superiority of the XOR (3T) based full adder designs in term of delay, power and power delay product (PDP) compared to the other full adder circuits. Simulation results illustrate the superiority of the designed adder circuits against the conventional CMOS, TG and Hybrid full adder circuits in terms of power, delay and power delay product (PDP).

KEYWORDS

Hybrid full adder, XOR-XNOR circuit, High Speed, Low Power, Very Large Scale Integrated (VLSI)Circuits.

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Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate

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ABSTRACT

In present work a new XNOR gate using three transistors has been presented, which shows power dissipation of 550.7272µW in 0.35µm technology with supply voltage of 3.3V. Minimum level for high output of 2.05V and maximum level for low output of 0.084V have been obtained. A single bit full adder using eight transistors has been designed using proposed XNOR cell, which shows power dissipation of 581.542µW. Minimum level for high output of 1.97V and maximum level for low output of 0.24V is obtained for sum output signal. For carry signal maximum level for low output of 0.32V and minimum level for high output of 3.2V have been achieved. Simulations have been performed by using SPICE based on TSMC 0.35µm CMOS technology. Power consumption of proposed XNOR gate and full adder has been compared with earlier reported circuits and proposed circuit's shows better performance in terms of power consumption and transistor count.

KEYWORDS

CMOS, exclusive-OR (XOR), exclusive-NOR (XNOR), full adder, low power, pass transistor logic.

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Arithmetic Operations in Multi-Valued Logic

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ABSTRACT

This paper presents arithmetic operations like addition, subtraction and multiplications in Modulo-4 arithmetic, and also addition, multiplication in Galois field, using multi-valued logic (MVL). Quaternary to binary and binary to quaternary converters are designed using down literal circuits. Negation in modular arithmetic is designed with only one gate. Logic design of each operation is achieved by reducing the terms using Karnaugh diagrams, keeping minimum number of gates and depth of net in to consideration. Quaternary multiplier circuit is proposed to achieve required optimization. Simulation result of each operation is shown separately using Hspice.

KEYWORDS

Multiple-valued logic, Quaternary logic, Modulo-n addition and multiplication, Galois addition and multiplication.

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Design of Reversible Sequential Circuit Using Reversible Logic Synthesis

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ABSTRACT

Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic.The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. In this paper, we have proposed a new reversible gate. And we have designed RS flip flop and D flip flop by using our proposed gate and Peres gate. The proposed designs are better than the existing proposed ones in terms of number of reversible gates and garbage outputs. So, this realization is more efficient and less costly than other realizations.

KEYWORDS

Reversible logic, Reversible gate, Power dissipation, Flip-Flop, Garbage, BME gate.

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Analog VLSI Implementation of Neural Network Architecture for Signal Processing

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ABSTRACT

With the advent of new technologies and advancement in medical science we are trying to process the information artificially as our biological system performs inside our body. Artificial intelligence through a biological word is realized based on mathematical equations and artificial neurons. Our main focus is on the implementation of Neural Network Architecture (NNA) with on a chip learning in analog VLSI for generic signal processing applications. In the proposed paper analog components like Gilbert Cell Multiplier (GCM), Neuron activation Function (NAF) are used to implement artificial NNA. The analog components used are comprises of multipliers and adders' along with the tan-sigmoid function circuit using MOS transistor in subthreshold region. This neural architecture is trained using Back propagation (BP) algorithm in analog domain with new techniques of weight storage. Layout design and verification of the proposed design is carried out using Tanner EDA 14.1 tool and synopsys Tspice. The technology used in designing the layouts is MOSIS/HP 0.5u SCN3M, Tight Metal.

KEYWORDS

Neural Network Architecture, Back Propagation Algorithm.

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Cell Stability Analysis of Conventional 6T Dynamic 8T SRAM Cell in 45NM Technology

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ABSTRACT

A SRAM cell must meet requirements for operation in submicron/nano ranges. The scaling of CMOS technology has significant impact on SRAM cell -- random fluctuation of electrical characteristics and substantial leakage current. In this paper we present dynamic column based power supply 8T SRAM cell and comparing the proposed SRAM cell with respect to conventional SRAM 6T in various aspects. To verify read stability and write ability analysis we use N-curve metric. Simulation results affirmed that proposed 8T SRAM cell achieved improved read stability, read current, and leakage current in 45nm Technology comparing with conventional 6T SRAM using cadence virtuoso tool.

KEYWORDS

SRAM, Leakage Current, N-curve, Read stability, Write-ability, Cadence, Virtuoso, 45nm Technology.

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Wishbone Bus Architecture - A Survey and Comparison

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ABSTRACT

The performance of an on-chip interconnection architecture used for communication between IP cores depends on the efficiency of its bus architecture. Any bus architecture having advantages of faster bus clock speed, extra data transfer cycle, improved bus width and throughput is highly desirable for a low cost, reduced time-to-market and efficient System-on-Chip (SoC). This paper presents a survey of WISHBONE bus architecture and its comparison with three other on-chip bus architectures viz. Advanced Microcontroller Bus Architecture (AMBA) by ARM, CoreConnect by IBM and Avalon by Altera. The WISHBONE Bus Architecture by Silicore Corporation appears to be gaining an upper edge over the other three bus architecture types because of its special performance parameters like the use of flexible arbitration scheme and additional data transfer cycle (Read-Modify-Write cycle). Moreover, its IP Cores are available free for use requiring neither any registration nor any agreement or license.

KEYWORDS

SoC buses, WISHBONE Bus, WISHBONE Interface.

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A New Approach to Design Low Power CMOS Flash A/D Converter

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ABSTRACT

In the present paper, a 4-bit flash analog to digital converter for low power SoC application is presented.CMOS inverter has been used as a comparator and by adjusting the ratio of channel width and length, the switching threshold of the CMOS inverter is varied to detect the input analog signal. The simulation results show that this proposed 4-bit flash ADC consumes about 12.4 mW at 200M sample/s with 3.3V supply voltage in TSMC 0.35 µm process. Compared with the traditional flash ADC, this proposed method can reduce about 78% in power consumption.

KEYWORDS

CMOS Inverter, XOR gate based encoder, Flash ADC.

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