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EVALUATION OF ATM FUNCTIONING USING VHDL AND FPGA

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ABSTRACT

It has been almost four decades that banks and other financial organizations have been gradually computerised, in order to improve service and efficiency and to reduce cost. The birth of Electronic Fund Transfer and Automated Teller Machines has given rise to 24-hour banking and a greater variety of services for the customer. This method uses a computer to transfer debits and credits, with the help of electronic pulses, which are carried through wires either to a magnetic disk or tape. ATM (Automated Teller Machine) has become an important part in our daily lives. People use ATM for various purposes such as money withdrawal, checking balance, changing password etc. Since it mainly deals with people's money, it has to be a secure system on which we can rely. We have taken a step towards increasing this security and integrity by trying to implement the functioning of an ATM using VLSI-based programming, HDL(Hardware Description Language).The conventional coding languages such as C,C++ are replaced by VHDL(Very High Speed Integrated Circuit Hardware Description Language) so that the code cannot be easily hacked or changed. This article consists of an insight into the various functions that can be performed using an ATM, a brief description of the Coding and the obtained simulation results. It also consists of the implementation of the code using FPGA Kit (Spartan3; Model no.-XC 3S50).

KEYWORDS

ATM (Automated Teller Machine), Security, HDL (Hardware Description Language), FPGA (Field Programmable Gate Array).

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DESIGN AND PERFORMANCE ANALYSIS OF HYBRID ADDERS FOR HIGH SPEED ARITHMETIC CIRCUIT

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ABSTRACT

Adder cells using Gate Diffusion Technique (GDI) & PTL-GDI technique are described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Performance comparison with various Hybrid Adder is been presented. In this paper, we propose two new designs based on GDI & PTL techniques, which is found to be much more power efficient in comparison with existing design technique. Only 10 transistors are used to implement the SUM & CARRY function for both the designs. The SUM and CARRY cell are implemented in a cascaded way i.e. firstly the XOR cell is implemented and then using XOR as input SUM as well as CARRY cell is implemented. For Proposed GDI adder the SUM as well as CARRY cell is designed using GDI technique. On the other hand in Proposed PTL-GDI adder the SUM cell is constructed using PTL technique and the CARRY cell is designed using GDI technique. The advantages of both the designs are discussed. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment.

KEYWORDS

GDI, PTL, PDP, low power, Full Adder & VLSI.

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REFERENCES

- [1] Monico Linares Aranda, Ramon Báez, Oscar Gonzalez Diaz, “Hybrid Adders for High-Speed Arithmetic Circuits A Comparison”. 7th International Conference on Electrical Engineering, Computing Science and Automatic Control, Sep 2010.
- [2] Sundeeppkumar Agarwal, Pavankumar V K, Yokesh R., “Energy –Efficient, High Performance Circuits for Arithmetic Units”. 21st International Conference on VLSI Design, pp. 371-376, 2008.
- [3] C.-H. Chang, J. Gu, and M. Zhang, “A review of 0.18nm full adder performances for tree structured arithmetic circuits,” IEEE Trans. Very Large Scale Integration Systems., vol. 13, no. 6, pp. 686–695, Jun. 2005..
- [4] Sumeer Goel, Ashok Kumar and Magdy A. Bayoumi, “Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style,” IEEE Trans. Very Large Scale Integration. Systems, vol. 14, no.12, pp.1309–1321, Dec. 2006.
- [5] RADHAKRISHNAN, D., “Low-voltage low-power CMOS full adder,” IEEE Proc. Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.
- [6] RADHAKRISHNAN, D., WHITAKER, S.R., and MAKI, G.K. “Formal design procedures for pass transistor switching circuits”, IEEE J. Solid-State Circuits, 1985, SC-20, pp. 53 1-536
- [7] RADHAKRISHNAN, D. “Design of CMOS circuits” IEEE Proc. Circuits Devices Syst., 1991, 138, (I),p p. 83-90
- [8] PEDRON, C., and STAUFFER, A. “Analysis and synthesis of combinational Circuits”, IEEE Trans. Commit.-Aided Des. Integr. Circuits Syst. 1988, 7, (7), pp. 775-786
- [9] Morgenshteid, A., Fish, A., and Wagner, I., A. “Gate-Diffusion Input (GDI) - a novel power efficient method for digital circuits: a design methodology” IEEE 2001
- [10]Nishad, A., K., Chandel, C., “Analysis of Low Power High Performance XOR Gate using GDI Technique”, IEEE Computer Society- International Conference on Computational Intelligence and Communication Systems, 2011
- [11]K. Navi, M. Reza Saatchi, O. Daei, “A High-speed hybrid full adder”, European Journal of Scientific Research, vol. 26, no. 1, pp.29-33, 2009
- [14]M. Aguirre and M. Linares, “An Alternative Logic Approach to Implement High-Speed Low-Power Full Adder Cells”, Brazilian Symposium on Integrated Circuit Design, pp. 166-171, Sep. 2005.
- [15]Mariano Aguirre-Hernandez and Monico Linares-Aranda “CMOS Full-Adders for Energy-Efficient Arithmetic Applications”, IEEE Transactions on VLSI Systems, In Press. 2010.

Area, Delay and Power Comparison of Adder Topologies

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Abstract

Adders form an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the pertinent choice for selecting the adder topology with the tradeoff between delay, power consumption and area. The adder topology used in this work are ripple carry adder, carry lookahead adder, carry skip adder, carry select adder, carry increment adder, carry save adder and carry bypass adder. The module functionality and performance issues like area, power dissipation and propagation delay are analyzed at 0.12μm 6metal layer CMOS technology using microwind tool.

Keywords

Ripple Carry Adder, Carry Save Adder, Carry Increment Adder, Carry Select Adder.

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REFERENCES

- [1] Animulislam, M.W. Akram, S.D. pable ,Mohd. Hasan, “Design and Analysis of Robust Dual Threshold CMOS Full Adder Circuit in 32 nm Technology”, International Conference on Advances in Recent Technologies in Communication and Computing,2010.
- [2] Deepa Sinha, Tripti Sharma, k.G.Sharma, Prof.B.P.Singh, “Design and Analysis of low Power 1-bit Full Adder Cell”,IEEE, 2011.
- [3] Nabihah Ahmad, Rezaul Hasan, “A new Design of XOR-XNOR gates for Low Power application”, International Conference on Electronic Devices, Systems and Applications(ICEDSA) ,2011.
- [4] R.Uma, “4-Bit Fast Adder Design: Topology and Layout with Self-Resetting Logic for Low Power VLSI Circuits”, International Journal of Advanced Engineering Sciences and Technology, Vol No. 7, Issue No. 2, 197 – 205.
- [5] David J. Willingham and izzet Kale, “A Ternary Adiabatic Logic (TAL) Implementation of a FourTrit Full-Adder,IEEE, 2011.
- [6] Padma Devi, Ashima Girdher and Balwinder Singh, “Improved Carry Select Adder with Reduced Area and Low Power Consumption”, International Journal of Computer Application,Vol 3.No.4, June 2010 .
- [7] B.Ramkumar, Harish M Kittur, P.Mahesh Kannan, “ASIC Implementation of Modified Faster Carry Save Adder”, European Journal of Scientific Research ISSN 1450-216X Vol.42 No.1, pp.53-58,2010.
- [8] Y. Sunil Gavaskar Reddy and V.V.G.S.Rajendra Prasad, “Power Comparison of CMOS and Adiabatic Full Adder Circuits”, International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011
- [9] Mariano Aguirre-Hernandez and Monico Linares-Aranda, “CMOS Full-Adders for Energy-Efficient Arithmetic Applications”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 4, April 2011.
- [10] Ning Zhu, Wang Ling Goh, Weija Zhang, Kiat Seng Yeo, and Zhi Hui Kong, “Design of Low-Power High-Speed Truncation-Error-Tolerant Adder and Its Application in Digital Signal Processing”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 18, No. 8, August 2010.
- [11] Sreehari Veeramachaneni, M.B. Srinivas, “New Improved 1-Bit Full Adder Cells”, IEEE, 2008.
- [12] Tripti Sharma, k.G.Sharma, Prof.B.P.Singh, Neha Arora, “High Speed, Low Power 8T Full Adder Cell with 45% Improvement in Threshold Loss Problem”, Recent Advances in Networking, VLSI and Signal Processing.
- [13] G.Shyam Kishore, “A Novel Full Adder with High Speed Low Area”, 2nd National Conference on Information and Communication Technology (NCICT) 2011 Proceedings published in International Journal of Computer Applications® (IJCA).

- [14] Shubhajit Roy Chowdhury, Aritra Banerjee, Aniruddha Roy, Hiranmay Saha, "A high Speed 8 Transistor Full Adder Design using Novel 3 Transistor XOR Gates", International Journal of Electrical and Computer Engineering 3:12 2008.
- [15] Romana Yousuf and Najeeb-ud-din, "Synthesis of Carry Select Adder in 65 nm FPGA", IEEE. [16] Shubin.V.V, "Analysis and Comparison of Ripple Carry Full Adders by Speed", Micro/Nano Technologies and Electron Devices(EDM),2010, International Conference and Seminar on, pp.132-135,2010.
- [17] Pudi. V, Sridhara., K, "Low Complexity Design of Ripple Carry and Brent Kung Adders in QCA", Nanotechnology, IEEE transactions on, Vol.11, Issue.1, pp.105-119, 2012.
- [18] Jian-Fei Jiang; Zhi-Gang Mao; Wei-Feng He; Qin Wang, "A New Full Adder Design for Tree Structured Arithmetic Circuits", Computer Engineering and Technology(ICCET),2010,2nd International Conference on, Vol.4, pp.V4-246-V4- 249,2010.

SINGLE ELECTRON TRANSISTOR: APPLICATIONS & PROBLEMS

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ABSTRACT

The goal of this paper is to review in brief the basic physics of nanoelectronic device single-electron transistor [SET] as well as prospective applications and problems in their applications. SET functioning based on the controllable transfer of single electrons between small conducting "islands". The device properties dominated by the quantum mechanical properties of matter and provide new characteristics coulomb oscillation, coulomb blockade that is helpful in a number of applications. SET is able to shear domain with silicon transistor in near future and enhance the device density. Recent research in SET gives new ideas which are going to revolutionize the random access memory and digital data storage technologies.

Keywords

Nanoelectronics; Single-electron transistor; Coulomb blockade, Coulomb oscillation, Quantum dot

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REFERENCES

- [1] M. A. Kastner, "The single electron transistor and artificial atoms", *Ann. Phys. (Leipzig)*, vol. 9, pp. 885-895, 2000.
- [2] S. Bednarek, B. Szafran, and J. Adamowski, "Solution of the Poisson Schrodinger problem for a single-electron transistor", *Phys. Rev. B*, Vol. 61, pp. 4461-4464, 2000.
- [3] Songphol Kanjanachuchai and Somsak Panyakeow, "Beyond CMOS: Single-Electron Transistors", *IEEE International Conference on Industrial Technology*, Bangkok, Thailand, 2002.
- [4] Masumi Saitoh, Hidehiro Harata and Toshiro Hiramoto, "Room-Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching", *IEEE International Electron Device Meeting*, San Francisco, USA, 2004.
- [5] K. Matsumoto, M. Ishii, K. Segawa, Y. Oka B. J. Vartanian and J. S. Harris, "Room temperature operation of a single electron transistor made by the scanning tunneling microscope nano oxidation process for the TiOx/Ti system", *Appl. Phys. Lett.* 68 (1), pp. 34-36, 1996.
- [6] Ken Uchida, Jugli Kaga, Ryuji Ohba and Akira Toriumi, "Programmable Single-Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room-Temperature Operation", *IEEE Transactions on Electron Devices*, Vol. 50, No. 7, July 2003.
- [7] T.A. Fulton and G.D. Dolan, "Observation of single electron charging effect in small tunnelling junction", *Phys. Rev. Lett.*, Vol. 59, pp. 109-112, July 1987.
- [8] Lingjie Guo, Effendi Leobandung and Stephen Y. Chou, "A silicon Single-Electron transistor Memory operating at room temperature", *Science* Vol. 275, pp. 649-651, 1997.
- [9] A.N. Cleand, D. Estene, C. Urbina and M.H. Devoret, "An extremely Low noise Photodetector based on the single electron Transistor" , *Journal of Low Temperature Physics*, Vol. 93, Nos. 3/4, pp.767-772, 1993.
- [10] R. Knobel, C.s. Yung and A.N. Cleland, "Single -electron transistor as a radio frequency mixer" , *Applied Physics Letters*, Vol. 81, No. 3, pp. 532-534, July 2002.

TRANSISTOR LEVEL IMPLEMENTATION OF DIGITAL REVERSIBLE CIRCUITS

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ABSTRACT

Now a days each and every electronic gadget is designing smartly and provides number of applications, so these designs dissipate high amount of power. Reversible logic is becoming one of the best emerging design technologies having its applications in low power CMOS, Quantum computing and Nanotechnology. Reversible logic plays an important role in the design of energy efficient circuits. Adders and subtractors are the essential blocks of the computing systems. In this paper, reversible gates and circuits are designed and implemented in CMOS and pass transistor logic using Mentor graphics backend tools. A four-bit ripple carry adder/subtractor and an eight-bit reversible Carry Skip Adder are implemented and compared with the conventional circuits.

KEYWORDS

Low power, Reversible logic gates, Adder, Subtractor, Mentor graphics tools.

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REFERENCES

- [1] R.Landauer, "Irreversibility and heat generation in the computational Process", IBM Research and Development, pp. 183-191, 1961.
- [2] C.H Bennett "Logical Reversibility of computations" IBM J. Research and development, pp 525-532, November-1973.
- [3] Raghava Garipelly, P.MadhuKiran, A.Santhosh Kumar "A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2013, pp.417-423.
- [4] Rashmi S.B, Tilak B G, Praveen B "Transistor Implementation of Reversible PRT Gates" International Journal of Engineering Science and Technology (IJEST) Vol. 3 No. 3 March 2011, pp.2289-2297.
- [5] Aakash Gupta, Pradeep Singla, Jitendra Gupta and Nitin Maheshwari, "An Improved Structure of Reversible Adder And Subtractor", International Journal of Electronics and Computer Science Engineering Volume 2, Number 2, pp.712-718.
- [6] A.Kamaraj , I.Vivek Anand , P.Marichamy, "Design of Low Power Combinational Circuits using Reversible Logic and Realization in Quantum Cellular Automata" International Journal of Innovative Research in Science, Engineering and Technology, Volume 3, Special Issue 3, March 2014, pp.1449- 1456.
- [7] V.Kamalakannan, Shilpakala.V, Ravi.H.N, "Design of Adder / Subtractor Circuits Based on Reversible Gates" Ijareeie, Vol. 2, Issue 8, August 2013, pp.3796-3804.
- [8] Rangaraju H G, Venugopal U, Muralidhara K N and Raja K B, "Low Power Reversible Parallel Binary Adder/ Subtractor".
- [9] M.SinghSankhwar "Design of High Speed Low Power Reversible Adder Using HNG Gate", International Journal of Engineering Research and Applications, Vol. 4, Issue 1 (Version 2), January 2014, pp.152-159.
- [10] D. P. Bala Subramanian, K.Kalaikaviya and S.Tamilselvan, "Low-Geometry High Speed Feynman Toffoli 8 Bit Carry Skip Adder", Journal of Global Research in Electronics and Communication Volume 1, No. 1, November-December 2012, pp. 6-9.
- [11] P. K. Lala, J.P. Parkerson, P. Chakraborty, "Adder Designs using Reversible Logic Gates ", WSEAS Transactions on Circuits And Systems, Volume 9, Issue 6, June 2010, pp. 369-378.
- [12] HimanshuThapliyal, A.P Vinod "Transistor Realization of Reversible TSG Gate and Reversible Adder Architectures", IEEE Asia Pacific Conference on Circuits and Systems, APCCAS 2006, pp.418-421.

DESIGN AND NOISE OPTIMIZATION OF RF LOW NOISE AMPLIFIER FOR IEEE STANDARD 802.11A WLAN

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ABSTRACT

Low noise amplifier is the front end block of radio-frequency receiver system. Its design required various characteristics such as power gain, noise figure, insertion losses and power consumption. In this paper we have proposed a single stage low noise amplifier design with high gain and low noise using inductive source degeneration topology for frequency range of 3 GHz to 7 GHz and also use the active biasing devices. A range of devices like inductors and capacitors are used to achieve 50 Ω input impedance with a low noise factor. The design process is simulated process is using Advance Design System (ADS) and implemented in TSMC 0.18 μm CMOS technology. A single stage low noise amplifier has a measured forward gain 25.4 dB and noise figure 2.2 dB at frequency 5.0 GHz.

KEYWORDS

Advanced design system, Low noise amplifier, Radio-frequency, Noise figure, Wireless network, CMOS, RF

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REFERENCES

- [1] Wei Guo and Daquan Huang, "The noise and linearity optimization for 1.9 GHz CMOS low Noise Amplifier," Proc. of IEEE Asia Pacific Conf. on ASIC, Taipei, Taiwan, 6-8 Aug. 2002, pp. 253-257.
- [2] Hsieh Hung Hsieh, "A 40 GHz low noise amplifier with a positive-feedback network in 0.18 μm CMOS," IEEE Trans. on Microwave Theory and Techniques, vol. 57, no. 8, pp. 1895-1902, Aug. 2009.
- [3] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of doublegate MOSFET over single-gate MOSFET for RF switch," Microelectronics Journal, vol. 42, no. 3, pp. 527-534, March 2011.
- [4] Nazif Emran Farid, Arjuna Marzuki, and Ahmad Ismat, "A variable gain 2.5 GHz CMOS low noise amplifier for mobile wireless communications," Proc. of 9th IEEE Int. Conf. of communications, Kuala Lumpur, Malaysia, 15-17 Dec. 2009, pp. 885-889.
- [5] Ming Hsien Tsai, S. Hsu, Fu Lung Hsueh, Chewn Pu Jou, Sean Chen, and Ming Hsiang, "A wideband low noise amplifier with 4 kV HBM ESD protection in 65 nm RF CMOS," IEEE Microwave and Wireless Components Letters, vol. 19, no. 11, pp. 734-736, Nov. 2009.
- [6] Bo Huang, Chi Hsueh Wang, Chung Chun Chen, Ming Fong Lei, Pin Cheng Huang, Kun You Lin, and Huei Wang, "Design and analysis for a 60 GHz low noise amplifier with RF ESD protection," IEEE Trans. on Microwave Theory and Techniques, vol. 57, no. 2, pp. 298-305, Feb. 2009.
- [7] Yu Lin Wei and Jun De Jin, "A low power low noise amplifier for K-band applications," IEEE Microwave and Wireless Components Letters, vol. 19, no. 2, pp. 116-118, Feb. 2009.
- [8] Bonghyuk Park, Sangsung Choi, and Songcheol Hong, "A low noise amplifier with tunable interference rejection for 3.1 to 10.6 GHz UWB systems," IEEE Microwave and Wireless Components Letters, vol. 20, no. 1, pp. 40-42, Jan 2010.
- [9] A. Meamar, Boon Chirn Chye, Man Anh, and Yeo Kiat Seng, "A 3 to 8 GHz low noise CMOS amplifier," IEEE Microwave and Wireless Components Letters, vol. 19, no. 4, pp. 245-247, April 2009.
- [10] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Analysis of double gate CMOS for double-pole four-throw RF switch design at 45-nm technology," J. of Computational Electronics, vol. 10, no. 1-2, pp. 229-240, June 2011.
- [11] Hyung Jin Lee, Dong Sam Ha, and Sang S. Choi, "A systematic approach to CMOS low noise amplifier design for ultra wideband applications," Proc. of Int. Symp. on Circuit and System, Kobe, Japan, 23-26 May 2005, pp. 3962-3965.
- [12] Wei Chang Li, Chao Shiun Wang, and Chorng Kuang Wang, "A 2.4 GHz/3.55 GHz/5 GHz multiband LNA with complementary switched capacitor multi-tap inductor in 0.18 μm CMOS," IEEE National Science Council (NSC) Taiwan, 2006, pp.1-4.
- [13] Roee Ben Yishay, Sara Stolyarova, Shye Shapira, Moshe Musiya, David Kryger, Yossi Shiloh, and Yael Nemirovsky, "A CMOS low noise amplifier with integrated front-side micro-machined inductor," Microelectronics Journal, vol. 42, no. 5, pp. 754-757, May 2011.

- [14] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge Univ. Press, 2nd Ed., 2004.
- [15] Nam Jin, "A low power 3.1–10.6 GHz ultra wide band CMOS low noise amplifier with common gate input stage," *Current Applied Physics*, vol. 11, no. 1, pp. 87-92, Jan. 2011.
- [16] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Capacitive model and S-parameters of doublepole four-throw double-gate RF CMOS switch," *Int. J. of Wireless Engineering and Technology*, vol. 2, no. 1, pp. 15-22, Jan. 2011.
- [17] H. W. Chiu, "A 2.17 dB NF 5 GHz band monolithic CMOS LNA with 10 mW DC power consumption," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 3, pp. 813-824, March 2005.
- [18] Hsien Chin Chiu, Chia Shih Cheng, Hsuan Ling Kao, Jeffrey S. Fu, Qiang Cui, and Juin J. Liou, "A fully on-chip ESD protection UWB band low noise amplifier using GaAs enhancement-mode dualgateHEMT technology," *Microelectronics Reliability*, vol. 51, no. 12, pp. 2137-2142, Dec. 2011.
- [19] Yuan Gao, Yuanjin Zheng, and Ban Leong, "A 0.18 μm CMOS UWB LNA with 5 GHz interference rejection," *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.* Honolulu, Hawaii, USA, 3-5 June 2007, pp. 47-50.
- [20] Y. S. Wang and L. H. Lu, "5.7 GHz low power variable gain LNA in 0.18 μm CMOS," *Electronics Letters*, vol. 41, no. 2, pp. 66-68, Jan. 2005. [21] M. Kumarasamy, Chin Boon, and K. Nuntha Kumar, "A fully integrated variable gain 5.75 GHz LNA with on-chip active balun for WLAN," *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, 8- 10 June 2003, pp. 439-442. [22] Seon Myoung, Sang Cheon, and Jong Yook, "Low noise and high linearity LNA based on InGaP/GaAs HBT for 5.3 GHz WLAN," *European Gallium Arsenide and Other Semiconductor Application Symp. (EGAAS)*, Paris, 2005.
- [23] Hye Ryoung Kim and Sang Gug Lee, "A 5-GHz LNA for wireless LAN application based on 0.5 μm SiGeBiCMOS," *2002 IEEE 3rd Int. Conf. on Microwave and Millimeter Wave Technology*, 17-19 Aug. 2002, pp. 50-53.
- [24] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF switch," *Microelectronics Journal*, vol. 42, no. 10, pp. 1124-1135, Oct. 2011.
- [25] Mu Chun Wang, Hsin Chia Yang, and Yi Jhen Li, "Minimization of cascade low noise amplifier with 0.18 μm CMOS process for 2.4 GHz RFID applications," *Electronics and Signal Processing, Lecture Notes in Electrical Engineering*, vol. 97, pp. 571-578, 2011.
- [26] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Possibilities of HfO₂ for double-pole four-throw double-gate RF CMOS switch," *4th IEEE Int. Symp. on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE-2011)*, Beijing, China, 1-3 Nov. 2011, pp. 309- 312.

SURVEY ON POWER OPTIMIZATION TECHNIQUES FOR LOW POWER VLSI CIRCUIT IN DEEP SUBMICRON TECHNOLOGY

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ABSTRACT

CMOS technology is the key element in the development of VLSI systems since it consumes less power. Power optimization has become an overridden concern in deep submicron CMOS technologies. Due to shrink in the size of device, reduction in power consumption and over all power management on the chip are the key challenges. For many designs power optimization is important in order to reduce package cost and to extend battery life. In power optimization leakage also plays a very important role because it has significant fraction in the total power dissipation of VLSI circuits. This paper aims to elaborate the developments and advancements in the area of power optimization of CMOS circuits in deep submicron region. This survey will be useful for the designer for selecting a suitable technique depending upon the requirement.

KEYWORDS

leakage power, low power, voltage scaling, power gating, transistor stacking, adiabatic logic.

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REFERENCES

- [1] Varsha Bendre & Dr. A.K. Kureshi, (2015), "An Overview of Various Leakage Power Reduction Techniques in Deep Submicron Technologies", proceedings of International Conference on Computing Communication Control and Automation, pp 992 -998.
- [2] Ing-Chao-Lin, Chin-Hong-lin, & Kuan-Hui-li, (Jan 2013), "Leakage and aging optimization using Transmission gate-based technique", IEEE Transactions on Computer aided design of integrated circuits and systems, vol.32.
- [3] Deepak kumar & Naveen Tiwari (march 2015) "VLSI Designs for Low Power Applications", Intl J Engg Sci Adv Research, vol.no.1, pp 71 – 75.
- [4] Akanksha Dixit, (2016), "Transistor Leakage Mechanisms and Power Reduction Techniques in CMOS VLSI Design", International Journal of Advanced Research in Computer and Communication Engineering, Vol.5, pp 102 – 105.
- [5] N. B. Romli, K. N. Minhad, M. B. I. Reaz & Md. S. Amin "An Overview of Power Dissipation And Control Techniques in CMOS Technology", Journal of Engineering Science and Technology, Vol.3, pp.364 – 382
- [6] Qiaing Tong, Ken Choi & Jun Dong Cho (2014) "A Review on System Level Low Power Techniques". Proceedings of international SoC Design conference.
- [7] Chethan Sharma "Low Power at Different Levels of Vlsi Design and Clock Distribution Schemes" Int. J. Comp. Tech. Appl., Vol 2 (1), 88-93 ISSN: 2229-6093
- [8] Ambily Babu, (November-2014), "Power Optimization Techniques at Circuit and Device Level in Digital CMOS VLSI – A Review" International Journal of Engineering Research & Technology (IJERT) IJERT , Vol.3 Issue 11,
- [9] Sumitha Gupta & Sukanya Padave, (March 2016), "Power Optimization for Low Power VLSI Circuits" International Journal of Advanced Research in Computer Science and Software Engineering, Vol. 6, No.3, pp96 – 99.
- [10] P. Sreenivasulu, P. khadar khan, Dr. K. Srinivasa Rao & Dr. A. VinayaBabu (July 2013) "Power Scaling in CMOS Circuits by Dual Threshold Voltage Technique" International Journal of Engineering and Innovative Technology (IJEIT) Volume 3, Issue 1.
- [11] S. Narendra, S. Borkar, V. De, Antoniadis & A. Chandrakasan, (August 2001), "Scaling of Stack effect and its Application for Leakage Reduction," in proceedings of the International Symposium on Low Power Electronics and Design, pp.195-200
- [12] Jun Cheol Park & Vincent J. Mooney, (November 2006), "Sleepy Stack Reduction of Leakage Power", IEEE Transactions on Very Large-Scale Integration (VLSI) systems, vol. 14, No. 11, pp. 1250-1263.
- [13] Ajay Sharma (2004) "Reduction in CMOS Circuits using Self-Controlled Stacked Transistors", Proceedings of the 17th International Conference on VLSI Design (VLSID'04) IEEE.

- [14] Narendra Hanchate & N. Ranganathan, (2004), 'A New Technique for Leakage Reduction in CMOS Circuits using Self-Controlled Stacked Transistors', Proceedings of the 17th International Conference on VLSI Design (VLSID'04) IEEE.
- [15] Xin He Al-Kadry & S. Abdollahi, (2009), "Adaptive leakage control on body biasing for reducing power consumption in CMOS VLSI circuit", Quality of Electronic Design, , pp: 465 – 470.
- [16] Dushyant Kumar Soni & Ashish Hiradhar, (June 2015), "Dynamic Power reduction of synchronous digital design by using of efficient clock gating technique" International Journal of Engineering and Techniques, Volume 1 Issue 3.
- [17] V.Sri Sai Harsha & Aparna, (September 2015,) "Sub-Threshold Leakage Current Reduction Techniques In VLSI Circuits -A Survey", Int. Journal of Engineering Research and Applications. 5, Issue 9, (Part - 1) pp.28-32.
- [18] R. Sivakumar & D. Jothi, (December 2014), "Recent Trends in Low Power VLSI Design", International Journal of Computer and Electrical Engineering, Vol. 6, NO.6.
- [19] Bhuvana B P, Manohar B R & Kanchana Baskaran V S (2016) "Adiabatic Logic Circuits Using FinFETs and CMOS – A Review "International Journal of Engineering and Technology, Vol 8, No2, pp 1256 – 1270.
- [20] Preethi Bhati & Navaid Z. Rizvi, (2016), "Adiabatic Logic: An Alternative Approach to Low Power Applications ", International Conference on Electrical, Electronics, and Optimization Techniques, pp 4256 – 4260.
- [21] Y. Sunil Gavaskar Reddy, V.V.G.S. Rajendra Prasad, (2011), "Power Comparison of CMOS And Adiabatic Full Adder Circuits", International Journal of Scientific & Engineering Research Volume 2, Issue 9, pp 1-5

Design of a high frequency low voltage CMOS operational amplifier

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ABSTRACT

A method is presented in this paper for the design of a high frequency CMOS operational amplifier (OpAmp) which operates at 3V power supply using tsmc 0.18 micron CMOS technology. The OPAMP designed is a two-stage CMOS OPAMP followed by an output buffer. This Operational Transconductance Amplifier (OTA) employs a Miller capacitor and is compensated with a current buffer compensation technique. The unique behaviour of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at a high frequency. Designing of two-stage op-amps is a multi-dimensional-optimization problem where optimization of one or more parameters may easily result into degradation of others. The OPAMP is designed to exhibit a unity gain frequency of 2.02GHz and exhibits a gain of 49.02dB with a 60.50 phase margin. As compared to the conventional approach, the proposed compensation method results in a higher unity gain frequency under the same load condition. Design has been carried out in Tanner tools. Simulation results are verified using S-edit and W-edit.

KEYWORDS

CMOS Analog Circuit, Operational amplifier, Current Buffer Compensation, High Frequency, Low Voltage

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<https://aircconline.com/vlsics/V2N1/2111vlsics07.pdf>

REFERENCES

- [1] G. Palmisano and G. Palumbo, "A compensation strategy for two-stage CMOS OPAMPs based on current buffer,". IEEE trans. Circuits sys.I, Fundam. Theory Appl., vol. 44, no. 3 , pp. 257- 262, mar1997.
- [2] J. Mahattanakul, "Design procedure for two stage CMOS operational amplifier employing current buffer", IEEE trans. Circuits sys. II, Express Briefs, vol 52, no.11 nov 2005.
- [3] G. Palmisano, G. Palumbo and S. Pennisi "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial"; Analog Integrated Circuits and Signal Processing, 27, 179–189, 2001.
- [4] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 2002.
- [5] P.E. Allen and D.R. Holberg, CMOS Analog Circuit Design. Oxford University Press, 2002.
- [6] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE J. Solid-State Circuits, Vol. SC-18, pp. 629-633, Dec, 1983.
- [7] D.A Johns and K. Martin, Analog Integrated Circuit Design. New York Willey, 1997. [8] Kang Sung-Mo, Leblebici Yusuf, "CMOS Digital Integrated Circuits, Analysis and design", Tata McGraw-Hill Edition 2003, Third Edition
- [9] G. Palmisano and G. Palumbo "A Compensation Strategy for Two-Stage CMOS opamps Based on Current Buffer"; IEEE Transactions on circuits and systems—I: Fundamental theory and applications, Vol. 44, No. 3, March. 1997.
- [10] R. Jacob Baker, Harry W.Li, David E. Boyce: CMOS circuit design, layout and simulation; IEEE press series on microelectronic systems.
- [11] R. Castello, "CMOS buffer amplifier," in Analog Circuit Design, J.Huijsing, R. van der Plassche, and W. Sansen, Eds. Boston, MA: Kluwer Academic, 1993, pp. 113–138.
- [12] Gregorian R., and Temes, G.C. "Analog MOS Integrated Circuits for Signal Processing", John Wiley and Sons, 1986. [13] Huijsing J., Hogervorst R. and de Langen K., "Low-power low-voltage VLSI operational amplifier cells". IEEE Transactions on circuits and systems-II, 42, pp.841-852, nov-1995
- [14] G. Palmisano and G. Palumbo "A very efficient CMOS low voltage output stage" , IEEE Electronic Letters 31(21). pp 1830-1831, 1995
- [15] G. Palmisano and G. Palumbo and R. Salerno "CMOS output stages for low voltage power supply" IEEE Trans. On CAS part-II 47(2), pp 96-104, feb 2000
- [16] Yavari, M. and Shoaee, O. (2004) "Low-Voltage Low-Power Fast-Settling CMOS Operational Transconductance Amplifiers for Switched Capacitor Applications". IEEE Proceedings - Circuits Devices Systems p. 151.
- [17] Johns, D. A. and Martin, K. (1997) Analog Integrated Circuit Design John Wiley & Sons , New York, USA

- [18] Mahattanakul, J. and Chutichatuporn, J. (2005) "Design Procedure for Two-Stage CMOS OPAMP with Flexible Noise-Power Balancing Scheme". IEEE Transaction on Circuits and Systems-I: Regular Paper 52, pp. 1508-1514.
- [19] Pugliese, A. , Cappuccino, G. and Cocorullo, G. (2008) "Design Procedure for Settling Time Minimization in Three-Stage Nested Miller Amplifiers". IEEE Transaction on Circuits and Systems-II 55, pp. 1-5.
- [20] Turchetti, C. and Masetti, G. (1983) "A Macromodel for Integrated All-MOS Operational Amplifiers". IEEE Journal of Solid-State Circuits SC-18 , pp. 389-394.
- [21] Yang, H. C. and Allstot, D. J. (1990) "Considerations for Fast Settling Operational Amplifiers". IEEE Transactions on Circuits and Systems 37, pp. 326-334.
- [22] Yavari, M., Maghari, N. and Shoaie, O. (2005) "An Accurate Analysis of Slew Rate for Twostage CMOS Opamps". IEEE Transactions on Circuits and Systems - II: Express Briefs 52, pp. 164-167.
- [23] C. Makris and C. Toumazou, "Current-mode active compensation techniques," *Electron. Letters*, vol. 26, no. 21, pp. 1792–1794, Oct. 11, 1990.
- [24] R. Kr. Baruah, "Design of a low power low voltage CMOS opamp" , *International Journal of VLSI design & communication systems*, vol. 1, no. 1, mar-2010.
- [25] R.Gonzalez, B.M. Gordon, M.A Horowitz, "Supply and Threshold voltage scaling for low power CMOS", *IEEE journal of solid state Electronics*, Vol sc 32, No 8, June 1997.
- [26] Ehsan Kargaran, HojatKhosrowjerdi and Karim Ghaffarzadegan, "A 1.5 V High Swing UltraLow-Power Two Stage CMOS OP-AMP in 0.18 μm Technology. 2010 2nd International Conference on Mechanical and Electronics Engineering (ICMEE 2010).
- [27] Mohammad Taherzadeh-Sani and Anas A. Hamoui,"A 1-V Process-Insensitive Current Scalable Two-Stage Opamp With Enhanced DC Gain and Settling Behavior in 65-nm Digital CMOS", *IEEE Journal of Solid State Circuits*, Vol. 46, No. 3, Mar-2011.
- [28] Anshu Gupta and D.K. Mishra, R. Khatri," A Two Stage and Three Stage CMOS OPAMP with Fast Settling, High DC Gain and Low Power Designed in 180nm Technology", *Digital Object Identifier: 10.1109/CISIM.2010.5643497 (CISIM 2010)*, pp. 448 – 453, Nov.2010.

MULTISIM DESIGN AND SIMULATION OF 2.2GHz LNA FOR WIRELESS COMMUNICATION

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ABSTRACT

This paper presents the work done on the design and simulation of a high frequency low noise amplifier for wireless communication. The purpose of the amplifier is to amplify the received RF path of a wireless network. With high gain, high sensitivity and low noise using Bipolar Junction transistor (BJT). The design methodology requires analysis of the transistor for stability, proper matching, network selection and fabrication. The BJT transistor was chosen for the design of the LNA due to its low noise and good gain at high frequency. These properties were confirmed using some measurement techniques including Network Analyzer, frequency analyzer Probe and Oscilloscope for the simulation and practical testing of the amplifier to verify the performance of the designed High frequency Low noise amplifier. The design goals of noise figure of 0.52dB-0.7dB and bias conditions are $V_{cc} = 3.5\text{ V}$ and $I_{cc} = 55\text{ mA}$ to produce 16.8 dB gain across the 0.4–2.2GHz band.

KEYWORDS

Amplifier, Bipolar Junction Transistor, Stability, LNA, Fabrication, Multism

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<https://aircconline.com/vlsics/V5N4/5414vlsi05.pdf>

REFERENCES

- [1] Dixit, N.: Design And Performance Of Low Voltage, Low Noise 900MHz Amplifier, No. 43-51, Pp. 26,2006
- [2] A.O. Fadamiro¹ and E.O. Ogunti Design of a High Frequency and High Sensitive Low Noise Amplifier Asian Journal of Engineering and Technology (ISSN: 2321 – 2462) Volume 01– Issue 02, June 2013
- [3] Yu Lin Wei and Jun De Jin, “A low power low noise amplifier for K-band applications,” IEEE Microwave and Wireless Components Letters, vol. 19, no. 2, pp. 116-118, Feb. 2009
- [4] Bonghyuk Park, Sangsungs Choi, and Songcheol Hong, “A low noise amplifier with tunable interference rejection for 3.1 to 10.6 GHz UWB systems,” IEEE Microwave and Wireless Components Letters, vol. 20, no. 1, pp. 40-42, Jan 2010.
- [5] Mercer, S.: An Introduction to Low-Noise Amplifier Design, RF Design, Pp.4 2008
- [6] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, “Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF switch,” Microelectronics Journal, vol. 42, no. 10, pp. 1124-1135, Oct. 2011
- [7] Shouxian, M.: Dival Band Low Noise Amplifier Design For Bluetooth And Hiper Law Application. PhD Dissertation In Electrical and Electronics Engineering, Nanyang Technological University.2006
- [8] H. W. Chiu, “A 2.17 dB NF 5 GHz band monolithic CMOS LNA with 10 mW DC power consumption,” IEEE Trans. Microwave Theory Tech., vol. 53, no. 3, pp. 813-824, March 2005.
- [9] Aniket, P.J., Mahaya, S.P., Joshi, B.C.s, Design and Development of Low Noise Amplifier for RF/MW Receiver. Journal of Scientific Research, Vol.2 Issue 6.2013

EXTENDED K-MAP FOR MINIMIZING MULTIPLE OUTPUT LOGIC CIRCUITS

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ABSTRACT

Minimization of multiple output functions of a digital logic circuit is a classic research problem. Minimal circuit is obtained by using multiple Karnaugh Maps (K-map), one for each function. In this paper we propose a novel technique that uses a single Karnaugh Map for minimizing multiple outputs of a single circuit. The algorithm basically accumulates multiple K-Maps into a single K-Map. Finding minimal numbers of minterms are easier using our proposed clustering technique. Experimental results show that minimization of digital circuits where more than one output functions are involved, our extended K-Map approach is more efficient as compare to multiple K-Map approach.

KEYWORDS

Boolean Algebra, Karnaugh Map, Digital Logic Circuit, Clustering

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<https://aircconline.com/vlsics/V4N4/4413vlsi01.pdf>

REFERENCES

- [1] Boole G. (1954): An Investigation of the Laws of Thought. — New York: Dover Publications.
- [2] Shannon C.E. (1938): A symbolic analysis of relay and switching circuits. —Trans. AIEE, Vol. 57, No. 6, pp. 713–723.
- [3] Karnaugh M. (1953): The map method for synthesis of combinatorial logic circuits. — Trans. AIEE Comm. Electron., Vol. 72, No. 4, pp. 593–598.
- [4] McCluskey E. J. (1956), “Minimization of Boolean functions”, Bell System Tech. J., Vol. 35, No. 5, pp. 1417–1444.
- [5] Quine W. V. (1952), “The problem of simplifying truth tables”, Amer. Math. Month., Vol. 59, No. 8, pp. 521–531.
- [6] Petrick S. K. (1959), “On the minimization of Boolean functions”, Proc. Int. Conf. Information Processing, Paris: Unesco, pp. 422–423.
- [7] McCluskey E. J. (1965), “Introduction to the Theory of Switching Circuits”, New York, McGrawHill.
- [8] Biswas N. N. (1971), “Minimization of Boolean Functions”, IEEE Trans. on Computers, Vol. C-20, pp. 925-929.
- [9] Hong S. J., Cain R. G., Ostapko D. L. (1974), “MINI: A Heuristic Approach for Logic Minimization”, IBM Journal of Research and Development, Vol. 18, pp. 443-458.
- [10] Rhyne V. T., Noe P. S., McKinney M. H., and Pooch U.W. (1977) “A New Technique for the Fast Minimization of Switching Functions”, IEEE Trans. on Computers, Vol. C-26, pp. 757-764.