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EVALUATIONOFATMFUNCTIONINGUSINGVHDLANDFPGA

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ABSTRACT

Ithasbeenalmostfourdecadesthatbanksandotherfinancialorganizationshavebeengradually computerised,inordertoimproveserviceandefficiencyandtoreducecost.Thebirthof ElectronicFundTransferandAutomatedTellerMachineshasgivenriseto24-hourbankinganda greater variety of servicesfor the customer. This method uses a computer totransfer debits andcredits,withthehelpofelectronicpulses,whicharecarriedthroughwireseithertoamagnetic disk or tape.ATM(AutomatedTellerMachine)hasbecomeanimportant partinourdailylives.People use ATM for various purposes such as money withdrawal, checking balance, changing passwordetc.Sinceitmainlydealswithpeople'smoney,ithastobeasecuresystemonwhich we can rely. We have taken a step towards increasing this securityandintegritybytryingto implementthefunctioningofanATMusingVLSI-basedprogramming,HDL(HardwareDescription Language).TheconventionalcodinglanguagessuchasC,C++arereplacedbyVHDL(VeryHighSpeedIntegr atedCircuitHardwareDescriptionLanguage)sothatthecode cannotbeeasilyhackedorchanged.Thisarticleconsistsofaninsightintothevariousfunctions thatcanbeperformedusinganATM,abriefdescriptionoftheCodingandtheobtainedsimulationresults.Italso consists of the implementation of the code using FPGAKit (Spartan3; Model no.-XC 3S50).

KEYWORDS

ATM(AutomatedTellerMachine),Security,HDL(HardwareDescriptionLanguage),FPGA(Field Programmable Gate Array).

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DESIGNANDPERFORMANCEANALYSISOFHYBRIDADDERSFORHIGHSPEEDARITHMETIC CIRCUIT

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ABSTRACT

Adder cells using GateDiffusion Technique (GDI)& PTL-GDItechniqueare described in this paper.GDI technique allows reducingpower consumption, propagation delay and low PDP (powerdelayproduct)whereasPassTransistorLogic(PTL)reducesthecountoftransistorsusedto makedifferentlogicgates,byeliminatingredundanttransistors.PerformancecomparisonwithvariousHybridAdderisbeenpresented.Inthispaper,weproposetwonewdesignsbasedon GDI&PTLtechniques,whichisfoundtobemuchmorepowerefficientin comparisonwith existingdesign technique.Only10 transistorsareusedtoimplementtheSUM&CARRY functionfor boththedesigns.TheSUMand CARRYcellare implementedinacascadedwayi.e. firstlytheXORcellis implementedandthenusingXORasinputSUMaswellasCARRYcellis implemented.ForProposedGDI adder the SUM as well as CARRY cell is designed using GDI technique.OntheotherhandinProposedPTL-GDIaddertheSUMcellisconstructedusingPTLtechniqueandtheCARRYcellisdesignedusingGDItechnique.Theadvantagesofboththe designs are discussed. The significance ofthese designsis substantiated bythe simulationresults obtainedfrom CadenceVirtuoso180nm environment.

KEYWORDS

GDI,PTL,PDP,lowpower,FullAdder&VLSI.

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Area,DelayandPowerComparisonofAdderTopologies

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Abstract

Adders form an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the pertinent choice for selecting the adder topologywiththetradeoffbetweendelay, power consumptionand area.The addertopologyused in thisworkareripplecarryadder,carrylookaheadadder,carryskipadder,carryselectadder,carry increment adder, carrysaveadder and carry bypass adder. Themodule functionality and performance issues like area, powerdissipation andpropagation delay are analyzedat 0.12µm 6metal layerCMOStechnologyusingmicrowind tool.

Keywords

RippleCarryAdder,CarrySaveAdder,CarryIncrementAdder,CarrySelectAdder.

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SINGLEELECTRONTRANSISTOR:APPLICATIONS&PROBLEMS

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ABSTRACT

Thegoalof thispaperis to reviewinbrief thebasicphysicsof nanoelectronicdevicesingle-electrontransistor[SET]aswellasprospectiveapplicationsandproblemsintheirapplications. SET functioningbased onthecontrollabletransfer of single electrons between small conducting "islands". The device properties dominated by the quantum mechanical properties of matter and provide new characteristicscoulomboscillation, coulombblockade that ishelpfulina number of applications.SET is able to shear domain withsilicon transistor innear futureandenhance the device density. Recent research in SET gives new ideas which are going to revolutionize the randomaccessmemoryanddigitaldatastoragetechnologies.

Keywords

Nanoelectronics;Single-electrontransistor;Coulombblockade,Coulomboscillation,Quantumdot

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TRANSISTORLEVELIMPLEMENTATIONOFDIGITALREVERSIBLECIRCUITS

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ABSTRACT

Nowadayseachandeveryelectronicgadgetisdesigningsmartlyandprovidesnumberof applications,sothesedesignsdissipatehighamountofpower.Reversiblelogicisbecomingoneofthebest emerging design technologies having its applications in low power CMOS, Quantum computing and Nanotechnology. Reversible logic playsan important role inthe designofenergy efficientcircuits.Addersandsubtractorsaretheessentialblocksofthecomputingsystems.In thispaper,reversiblegatesandcircuitsaredesignedandimplementedinCMOSandpass transistorlogicusingMentorgraphicsbackendtools.Afour-bitripplecarryadder/subtractorandaneight-bitreversibleCarrySkipAdderareimplementedandcomparedwiththeconventional circuits.

KEYWORDS

Lowpower,Reversiblelogicgates,Adder,Subtractor,Mentorgraphicstools.

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DESIGNANDNOISEOPTIMIZATIONOFRFLOWNOISEAMPLIFIERFORIEEE STANDARD 802.11A WLAN

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ABSTRACT

Lownoiseamplifieristhefrontendblockofradio-frequencyreceiversystem.Itsdesignrequiredvariouscharacteristicssuchaspowergain,noisefigure,insertionlossesandpowerconsumption.
Inthispaperwehaveproposedasinglestagelownoiseamplifierdesignwithhighgainandlow noiseusinginductivesourcedegenerationtopologyforfrequencyrangeof3GHzto7GHzandalsousetheactive biasingdevices.Arangeofdeviceslikeinductorsandcapacitorsareusedtoachieve50 Ωinputimpedancewithalownoisefactor.Thedesignprocessissimulatedprocessisusing AdvanceDesignSystem(ADS)andimplementedinTSMC0.18µmCMOStechnology.Asingle stagelownoiseamplifierhasameasuredforwardgain25.4dBandnoisefigure2.2dBat frequency 5.0 GHz.

KEYWORDS

Advanceddesignsystem,Lownoiseamplifier,Radio-frequency,Noisefigure,Wirelessnetwork, CMOS, RF

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SURVEYONPOWEROPTIMIZATIONTECHNIQUESFORLOWPOWERVLSI CIRCUITINDEEPSUBMICRONTECHNOLOGY

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ABSTRACT

CMOStechnologyisthekeyelementinthedevelopmentofVLSIsystemssinceitconsumesless power. Power optimization has become an overridden concern in deep submicron CMOS technologies.Duetoshrinkin thesizeof device, reduction in powerconsumptionandover all power management on the chip are the key challenges. For many designs power optimization is importantinordertoreducepackagecostandtoextendbatterylife.Inpoweroptimizationleakagealsoplaysa very important role because it has significant fraction in the total power dissipationofVLSIcircuits.Thispaperaimstoelaboratethedevelopmentsandadvancementsin the area of power optimization of CMOScircuitsin deepsubmicron region. This survey willbe usefulforthedesignerforselectingasuitabletechniquedependinguponthe requirement.

KEYWORDS

leakagepower,lowpower,voltagescaling,powergating,transistorstacking,adiabaticlogic.

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DesignofahighfrequencylowvoltageCMOSoperationalamplifier

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ABSTRACT

AmethodispresentedinthispaperforthedesignofahighfrequencyCMOSoperational amplifier(OpAmp)whichoperatesat3Vpowersupplyusingtsmc0.18micronCMOS technology.TheOPAMPdesignedisatwo-stageCMOSOPAMPfollowedbyan outputbuffer. ThisOperationalTransconductanceAmplifier(OTA)employsaMillercapacitorandiscompensatedwitha current buffer compensation technique. The unique behaviour of the MOS transistorsinsaturationregionnotonlyallowsadesignertoworkatalowvoltage,butalsoata highfrequency.Designingoftwo-stageop-ampsisamulti-dimensional-optimizationproblem where optimizationofoneormoreparametersmayeasilyresultintodegradationofothers.The OPAMPisdesignedtoexhibitaunitygainfrequencyof2.02GHzandexhibitsagainof49.02dBwitha 60.50phasemargin.Ascomparedtotheconventionalapproach,theproposedcompensationmethodresultsin a higher unity gain frequency under the same load condition. Design hasbeen carriedoutinTannertools.Simulationresultsareverifiedusing S-editandW-edit.

KEYWORDS

CMOSAnalogCircuit,Operationalamplifier,CurrentBufferCompensation,HighFrequency,LowVoltage

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MULTISIMDESIGNANDSIMULATIONOF2.2GHzLNAFORWIRELESS COMMUNICATION

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ABSRACT

Thispaperpresentstheworkdoneonthedesignandsimulationofahighfrequencylownoise amplifierforwirelesscommunication.Thepurposeoftheamplifieristoamplifythereceived RF pathofa wirelessnetwork.Withhighgain,highsensitivityandlownoiseusingBipolarJunctiontransistor(BJT).Thed esignmethodologyrequiresanalysisofthetransistorforstability,propermatching,networkselectionandfabri cation.TheBJTtransistorwaschosenforthedesignofthe LNAduetoitslownoiseandgoodgainathighfrequency.Thesepropertieswereconfirmed using some measurementtechniquesincludingNetworkAnalyzer,frequencyanalyzerProbeandOscilloscope forthesimulationandpracticaltestingoftheamplifiertoverifytheperformanceofthedesignedHigh frequencyLownoiseamplifier. Thedesign goalsofnoisefigureof0.52dB-0.7dB andbiasconditionsareVcc=3.5VandIcc=55mAtoproduce16.8dBgainacrossthe0.4–2.2GHzband.

KEYWORDS

Amplifier,BipolarJunctionTransistor,Stability,LNA,Fabrication,Multism

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EXTENDEDK-MAPFORMINIMIZINGMULTIPLEOUTPUTLOGICCIRCUITS

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ABSTRACT

Minimization of multiple output functions ofa digital logic circuit isa classic research problem. Minimalcircuit isobtained byusing multiple KarnaughMaps(K-map),one for eachfunction. Inthis paper we propose a novel technique that uses a single Karnaugh Map for minimizing multiple outputsofasinglecircuit.Thealgorithm basicallyaccumulatesmultiple K-MapsintoasingleK- Map. Finding minimal numbers of mintermsare easier using our proposed clustering technique. Experimental results show that minimization of digital circuits where more than one output functionsareinvolved,our extended K-Mapapproachismoreefficientascomparetomultiple K- Map approach.

KEYWORDS

BooleanAlgebra,KarnaughMap,DigitalLogicCircuit,Clustering

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