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EVALUATION OF ATM FUNCTIONING USING VHDLANDFPGA

ManaliDhar[1],DebolinaRoy[2]andTamoshaSaha[3]

[1]AssistantProfessor,DepartmentofElectronics&CommunicationEngineering,DSCS DEC,Kolkata,India[2,3]UGStudent,DepartmentofElectronics&Communication Engineering, DSCSDEC, Kolkata, India

ABSTRACT

It hasbeenalmost four decadesthat banksand other financial organizationshave been gradually computerised,inordertoimproveserviceandefficiencyandtoreducecost.Thebirthof ElectronicFundTransferandAutomatedTellerMachineshasgivenriseto24-hourbankinganda greater variety of services for the customer. This method uses a computer totransfer debits andcredits,withthehelpofelectronicpulses,whicharecarriedthroughwireseithertoamagnetic disk or tape.ATM (AutomatedTeller Machine) has become an important part in our daily lives.People use ATM for various purposes such as money withdrawal, checking balance, changing passwordetc.Sinceitmainlydealswithpeople'smoney,ithastobeasecuresystemonwhich we can rely. We have taken a step towards increasing this security and integrity by trying to implementthefunctioningofanATMusingVLSI-basedprogramming,HDL(Hardware Description Language).The conventional coding languages such as C,C++ are replaced by VHDL(VeryHighSpeedIntegratedCircuitHardwareDescriptionLanguage)sothatthecode cannotbeeasilyhackedorchanged.Thisarticleconsistsofaninsightintothevariousfunctions thatcanbeperformedusinganATM,abriefdescriptionoftheCodingandtheobtained simulation results. It also consists of the implementation of the code using FPGAKit (Spartan3; Model no.-XC 3S50).

KEYWORDS

ATM(AutomatedTellerMachine),Security,HDL(HardwareDescriptionLanguage),FPGA(Field Programmable Gate Array).

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DESIGNANDPERFORMANCEANALYSISOFHYBRIDADDERSFORHIGHSPEEDARITHMETIC CIRCUIT

RajkumarSarma[1]andVeeratiRaju[2]

[1]SchoolofElectronicsEngineering,LovelyProfessionalUniversity,Punjab(India)

[2]DepartmentofVLSI,LovelyProfessionalUniversity,Punjab(India)

ABSTRACT

Adder cells using GateDiffusion Technique (GDI)& PTL-GDItechniqueare described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (powerdelayproduct)whereas PassTransistor Logic (PTL)reducesthe count oftransistors usedto makedifferentlogicgates,byeliminatingredundanttransistors.PerformancecomparisonwithvariousHybridAdderisbeenpresented.Inthispaper,weproposetwonewdesignsbasedon GDI& PTLtechniques,whichisfoundtobemuchmorepowerefficientin comparisonwith existingdesign technique.Only10 transistorsareusedtoimplementtheSUM&CARRY functionfor boththedesigns. TheSUMand CARRYcellare implemented inacascadedwayi.e. firstlytheXORcellis implementedandthenusing XORas input SUMaswellasCARRYcellis implemented. For Proposed GDI adder the SUM as well as CARRY cell is designed using GDI technique.OntheotherhandinProposedPTL-GDIaddertheSUMcellisconstructedusingPTLtechniqueandtheCARRYcellisdesignedusingGDItechnique.Theadvantagesofboththe designs are discussed. The significance ofthese designs is substantiated bythe simulationresults obtainedfrom CadenceVirtuoso180nm environment.

KEYWORDS

GDI,PTL,PDP,lowpower,FullAdder&VLSI.

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Area,DelayandPowerComparisonofAdderTopologies

[1]R.UMA,VidyaVijayan[2],M.Mohanapriya[2],Sharon

Paul[2][1]ResearchScholar,DepartmentofComputerSciencePondicherryUniversity, Pondicherry,India

[2]UGStudents,DepartmentofElectronicsandCommunicationEngineeringRajivGandhi CollegeofEngineeringandTechnologyPondicherry,India

Abstract

Adders form an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the pertinent choice for selecting the adder topologywiththetradeoffbetweendelay, power consumptionand area.The addertopologyused in thisworkaripplecarryadder,carrylookaheadadder,carryskipadder,carryselectadder,carry increment adder, carrysaveadder and carry bypass adder. Themodule functionality and performance issues like area, powerdissipation andpropagation delay are analyzedat 0.12µm 6metal layerCMOStechnologyusingmicrowind tool.

Keywords

RippleCarryAdder,CarrySaveAdder,CarryIncrementAdder,CarrySelectAdder.

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SINGLEELECTRONTRANSISTOR:APPLICATIONS&PROBLEMS

OmKumar1andManjitKaur2

[1,2]VLSI-ES,Department,CentreforDevelopmentofAdvancedComputing,Mohali,India

ABSTRACT

Thegoalof thispaperis to reviewinbrief thebasicphysicsof nanoelectronicdevicesingle-electrontransistor[SET]aswellasprospectiveapplicationsandproblemsintheirapplications. SET functioningbased onthecontrollabletransfer of single electrons between small conducting "islands". The device properties dominated by the quantum mechanical properties of matter and provide new characteristicscoulomboscillation, coulombblockade that ishelpfulina number of applications.SET is able to shear domain withsilicon transistor innear futureandenhance the device density. Recent research in SET gives new ideas which are going to revolutionize the randomaccessmemoryanddigitaldatastoragetechnologies.

Keywords

Nanoelectronics;Single-electrontransistor;Coulombblockade,Coulomboscillation,Quantumdot

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TRANSISTORLEVELIMPLEMENTATIONOFDIGITALREVERSIBLECIRCUITS

K.PrudhviRaj1andY.Syamala2

1PGstudent,GudlavalleruEngineeringCollege,Krishnadistrict,AndhraPradesh,India2Departement of ECE,Gudlavalleru engineering college, Krishna district, AndhraPradesh, India

ABSTRACT

Now a days each and every electronic gadget is designing smartly and provides number of applications,sothesedesigns dissipatehighamountofpower.Reversiblelogic is becomingone ofthe best emerging design technologies having its applications in low power CMOS, Quantum computing and Nanotechnology. Reversible logic playsan important role inthe designofenergy efficientcircuits.Addersandsubtractorsaretheessentialblocksofthecomputingsystems.In thispaper,reversiblegatesandcircuitsaredesignedandimplementedinCMOSandpass transistorlogicusingMentorgraphicsbackendtools.Afour-bitripplecarryadder/subtractorandaneight-bitreversibleCarrySkipAdderareimplementedandcomparedwiththeconventional circuits.

KEYWORDS

Lowpower,Reversiblelogicgates,Adder,Subtractor,Mentorgraphicstools.

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DESIGNANDNOISEOPTIMIZATIONOFRFLOWNOISEAMPLIFIERFORIEEE STANDARD 802.11A WLAN

RavinderKumar1,MunishKumar2,andViranjayM.Srivastava1

[1]DepartmentofElectronicsandCommunicationEngineering,JaypeeUniversityof InformationTechnology,Solan-173234,India.

[2]DepartmentofElectronicsandCommunicationEngineering,GuruJambheshwarUniversityof ScienceandTechnology,Hisar-125001,India

ABSTRACT

Lownoiseamplifieristhefrontendblockofradio-frequencyreceiversystem.Itsdesignrequiredvariouscharacteristicssuchaspowergain,noisefigure,insertionlossesandpowerconsumption.
Inthispaperwehaveproposedasinglestagelownoiseamplifierdesignwithhighgainandlow noiseusinginductivesourcedegenerationtopologyforfrequencyrangeof3GHzto7GHzandalsousetheactive biasingdevices.Arangeofdeviceslikeinductorsandcapacitorsareusedtoachieve50 Ωinputimpedancewithalownoisefactor.Thedesignprocessissimulatedprocessisusing AdvanceDesignSystem(ADS)andimplementedinTSMC0.18µmCMOStechnology.Asingle stagelownoiseamplifierhasameasuredforwardgain25.4dBandnoisefigure2.2dBat frequency 5.0 GHz.

KEYWORDS

Advanceddesignsystem,Lownoiseamplifier,Radio-frequency,Noisefigure,Wirelessnetwork, CMOS, RF

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SURVEYONPOWEROPTIMIZATIONTECHNIQUESFORLOWPOWERVLSI CIRCUITINDEEPSUBMICRONTECHNOLOGY

T.SugunaandM.JanakiRani

DepartmentofElectronicsandCommunicationEngineering,Dr.M.G.REducationaland ResearchInstitute,Chennai,India

ABSTRACT

CMOStechnologyisthekeyelementinthedevelopmentofVLSIsystemssinceitconsumesless power. Power optimization has become an overridden concern in deep submicron CMOS technologies.Duetoshrinkin thesizeof device, reduction in powerconsumptionandover all power management on the chip are the key challenges. For many designs power optimization is importantinordertoreducepackagecostandtoextendbatterylife.Inpoweroptimization leakage also plays a very important role because it has significant fraction in the total power dissipationofVLSIcircuits.Thispaperaimstoelaboratethedevelopmentsandadvancementsin the area of power optimization of CMOScircuitsin deepsubmicron region. This survey willbe usefulforthedesignerforselectingasuitabletechniquedependinguponthe requirement.

KEYWORDS

leakagepower,lowpower,voltagescaling,powergating,transistorstacking,adiabaticlogic.

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DesignofahighfrequencylowvoltageCMOSoperationalamplifier

Priyanka Kakoty

DepartmentofElectronicsandCommunicationEngineering,TezpurUniversity,India

ABSTRACT

AmethodispresentedinthispaperforthedesignofahighfrequencyCMOSoperational amplifier(OpAmp)whichoperatesat3Vpowersupplyusingtsmc0.18micronCMOS technology.TheOPAMPdesignedisatwo-stageCMOSOPAMPfollowedbyan outputbuffer. ThisOperationalTransconductanceAmplifier(OTA)employsaMillercapacitorandis compensated with a current buffer compensation technique. The unique behaviour of the MOS transistorsinsaturationregionnotonlyallowsadesignertoworkatalowvoltage,butalsoata highfrequency.Designingoftwo-stageop-ampsisamulti-dimensional-optimizationproblem where optimization of one or more parameters may easily result into degradation of others. The OPAMPisdesignedtoexhibitaunitygainfrequencyof2.02GHzandexhibitsagainof49.02dBwitha 60.50phasemargin.Ascomparedtotheconventionalapproach,theproposedcompensation method results in a higher unity gain frequency under the same load condition. Design has been carriedoutinTannertools.Simulationresultsareverifiedusing S-editandW-edit.

KEYWORDS

CMOSAnalogCircuit,Operationalamplifier,CurrentBufferCompensation,HighFrequency,LowVoltag e

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MULTISIMDESIGNANDSIMULATIONOF2.2GHzLNAFORWIRELESS COMMUNICATION

OluwajobiF.I,Lawalwasiu

DepartmentofElectrical/ElectronicEngineering,RUFUSGIWAPolytechnic,OWO,P.M.B1019,Nigeria

ABSRACT

This paper presents the work done on the design and simulation of a high frequency low noise amplifierforwirelesscommunication.ThepurposeoftheamplifieristoamplifythereceivedRF pathofa wireless network. Withhighgain, highsensitivityand low noise using Bipolar Junction transistor (BJT). The design methodology requires analysis of the transistor for stability, proper matching,networkselectionandfabrication.TheBJTtransistorwaschosenforthedesignofthe LNAduetoitslownoiseandgoodgainathighfrequency.Thesepropertieswereconfirmed using some measurement techniques including NetworkAnalyzer, frequencyanalyzer Probe and Oscilloscope forthe simulationand practicaltestingofthe amplifierto verifythe performance of the designed High frequencyLownoiseamplifier. Thedesign goalsofnoisefigureof0.52dB-0.7dB andbiasconditionsareVcc=3.5VandIcc=55mAtoproduce16.8dBgainacrossthe0.4–2.2GHzband.

KEYWORDS

Amplifier,BipolarJunctionTransistor,Stability,LNA,Fabrication,Multism

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EXTENDEDK-MAPFORMINIMIZINGMULTIPLEOUTPUTLOGICCIRCUITS

PalashDas[1],BikromadittyaMondal[2]

[1]DepartmentofComputerScienceandTechnology,BengalEngineeringandScienceUniversity, Shibpur, Howrah, India.

[2]DepartmentofComputerScienceandEngineering,BPPoddarInstituteofManagementand Technology,Kolkata,India.

ABSTRACT

Minimization of multiple output functions ofa digital logic circuit isa classic research problem. Minimalcircuit isobtained byusing multiple KarnaughMaps(K-map),one for eachfunction. Inthis paper we propose a novel technique that uses a single Karnaugh Map for minimizing multiple outputsofasinglecircuit.Thealgorithm basicallyaccumulatesmultiple K-MapsintoasingleK- Map. Finding minimal numbers of mintermsare easier using our proposed clustering technique. Experimental results show that minimization of digital circuits where more than one output functionsareinvolved,our extended K-Mapapproachismoreefficientascomparetomultiple K- Map approach.

KEYWORDS

BooleanAlgebra,KarnaughMap,DigitalLogicCircuit,Clustering

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