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EVALUATION OF ATM FUNCTIONING USING VHDL AND FPGA

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ABSTRACT

It has been almost four decades that banks and other financial organizations have been gradually computerised, in order to improve service and efficiency and to reduce cost. The birth of Electronic Fund Transfer and Automated Teller Machines has given rise to 24-hour banking and a greater variety of services for the customer. This method uses a computer to transfer debits and credits, with the help of electronic pulses, which are carried through wires either to a magnetic disk or tape. ATM (Automated Teller Machine) has become an important part in our daily lives. People use ATM for various purposes such as money withdrawal, checking balance, changing password etc. Since it mainly deals with people's money, it has to be a secure system on which we can rely. We have taken a step towards increasing this security and integrity by trying to implement the functioning of an ATM using VLSI-based programming, HDL(Hardware Description Language).The conventional coding languages such as C,C++ are replaced by VHDL(Very High Speed Integrated Circuit Hardware Description Language) so that the code cannot be easily hacked or changed. This article consists of an insight into the various functions that can be performed using an ATM, a brief description of the Coding and the obtained simulation results. It also consists of the implementation of the code using FPGA Kit (Spartan3; Model no.-XC 3S50).

KEYWORDS

ATM (Automated Teller Machine), Security, HDL (Hardware Description Language), FPGA (Field Programmable Gate Array).

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DESIGN AND PERFORMANCE ANALYSIS OF HYBRID ADDERS FOR HIGH SPEED ARITHMETIC CIRCUIT

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ABSTRACT

Adder cells using Gate Diffusion Technique (GDI) & PTL-GDI technique are described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Performance comparison with various Hybrid Adder is been presented. In this paper, we propose two new designs based on GDI & PTL techniques, which is found to be much more power efficient in comparison with existing design technique. Only 10 transistors are used to implement the SUM & CARRY function for both the designs. The SUM and CARRY cell are implemented in a cascaded way i.e. firstly the XOR cell is implemented and then using XOR as input SUM as well as CARRY cell is implemented. For Proposed GDI adder the SUM as well as CARRY cell is designed using GDI technique. On the other hand in Proposed PTL-GDI adder the SUM cell is constructed using PTL technique and the CARRY cell is designed using GDI technique. The advantages of both the designs are discussed. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment.

KEYWORDS

GDI, PTL, PDP, low power, Full Adder & VLSI.

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Area, Delay and Power Comparison of Adder Topologies

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Abstract

Adders form an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the pertinent choice for selecting the adder topology with the tradeoff between delay, power consumption and area. The adder topology used in this work are ripple carry adder, carry lookahead adder, carry skip adder, carry select adder, carry increment adder, carry save adder and carry bypass adder. The module functionality and performance issues like area, power dissipation and propagation delay are analyzed at 0.12µm 6metal layer CMOS technology using microwind tool.

Keywords

Ripple Carry Adder, Carry Save Adder, Carry Increment Adder, Carry Select Adder.

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SINGLE ELECTRON TRANSISTOR: APPLICATIONS & PROBLEMS

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ABSTRACT

The goal of this paper is to review in brief the basic physics of nanoelectronic device single-electron transistor [SET] as well as prospective applications and problems in their applications. SET functioning based on the controllable transfer of single electrons between small conducting "islands". The device properties dominated by the quantum mechanical properties of matter and provide new characteristics coulomb oscillation, coulomb blockade that is helpful in a number of applications. SET is able to shear domain with silicon transistor in near future and enhance the device density. Recent research in SET gives new ideas which are going to revolutionize the random access memory and digital data storage technologies.

Keywords

Nanoelectronics; Single-electron transistor; Coulomb blockade, Coulomb oscillation, Quantum dot

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TRANSISTOR LEVEL IMPLEMENTATION OF DIGITAL REVERSIBLE CIRCUITS

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ABSTRACT

Now a days each and every electronic gadget is designing smartly and provides number of applications, so these designs dissipate high amount of power. Reversible logic is becoming one of the best emerging design technologies having its applications in low power CMOS, Quantum computing and Nanotechnology. Reversible logic plays an important role in the design of energy efficient circuits. Adders and subtractors are the essential blocks of the computing systems. In this paper, reversible gates and circuits are designed and implemented in CMOS and pass transistor logic using Mentor graphics backend tools. A four-bit ripple carry adder/subtractor and an eight-bit reversible Carry Skip Adder are implemented and compared with the conventional circuits.

KEYWORDS

Low power, Reversible logic gates, Adder, Subtractor, Mentor graphics tools.

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DESIGN AND NOISE OPTIMIZATION OF RF LOW NOISE AMPLIFIER FOR IEEE STANDARD 802.11A WLAN

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ABSTRACT

Low noise amplifier is the front end block of radio-frequency receiver system. Its design required various characteristics such as power gain, noise figure, insertion losses and power consumption. In this paper we have proposed a single stage low noise amplifier design with high gain and low noise using inductive source degeneration topology for frequency range of 3 GHz to 7 GHz and also use the active biasing devices. A range of devices like inductors and capacitors are used to achieve 50 Ω input impedance with a low noise factor. The design process is simulated process is using Advance Design System (ADS) and implemented in TSMC 0.18 µm CMOS technology. A single stage low noise amplifier has a measured forward gain 25.4 dB and noise figure 2.2 dB at frequency 5.0 GHz.

KEYWORDS

Advanced design system, Low noise amplifier, Radio-frequency, Noise figure, Wireless network, CMOS, RF

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SURVEY ON POWER OPTIMIZATION TECHNIQUES FOR LOW POWER VLSI CIRCUIT IN DEEP SUBMICRON TECHNOLOGY

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ABSTRACT

CMOS technology is the key element in the development of VLSI systems since it consumes less power. Power optimization has become an overridden concern in deep submicron CMOS technologies. Due to shrink in the size of device, reduction in power consumption and over all power management on the chip are the key challenges. For many designs power optimization is important in order to reduce package cost and to extend battery life. In power optimization leakage also plays a very important role because it has significant fraction in the total power dissipation of VLSI circuits. This paper aims to elaborate the developments and advancements in the area of power optimization of CMOS circuits in deep submicron region. This survey will be useful for the designer for selecting a suitable technique depending upon the requirement.

KEYWORDS

leakage power, low power, voltage scaling, power gating, transistor stacking, adiabatic logic.

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Design of a high frequency low voltage CMOS operational amplifier

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ABSTRACT

A method is presented in this paper for the design of a high frequency CMOS operational amplifier (OpAmp) which operates at 3V power supply using tsmc 0.18 micron CMOS technology. The OPAMP designed is a two-stage CMOS OPAMP followed by an output buffer. This Operational Transconductance Amplifier (OTA) employs a Miller capacitor and is compensated with a current buffer compensation technique. The unique behaviour of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at a high frequency. Designing of two-stage op-amps is a multi-dimensional-optimization problem where optimization of one or more parameters may easily result into degradation of others. The OPAMP is designed to exhibit a unity gain frequency of 2.02GHz and exhibits a gain of 49.02dB with a 60.50 phase margin. As compared to the conventional approach, the proposed compensation method results in a higher unity gain frequency under the same load condition. Design has been carried out in Tanner tools. Simulation results are verified using S-edit and W-edit.

KEYWORDS

CMOS Analog Circuit, Operational amplifier, Current Buffer Compensation, High Frequency, Low Voltage

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MULTISIM DESIGN AND SIMULATION OF 2.2GHz LNA FOR WIRELESS COMMUNICATION

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ABSRACT

This paper presents the work done on the design and simulation of a high frequency low noise amplifier for wireless communication. The purpose of the amplifier is to amplify the received RF path of a wireless network. With high gain, high sensitivity and low noise using Bipolar Junction transistor (BJT). The design methodology requires analysis of the transistor for stability, proper matching, network selection and fabrication. The BJT transistor was chosen for the design of the LNA due to its low noise and good gain at high frequency. These properties were confirmed using some measurement techniques including Network Analyzer, frequency analyzer Probe and Oscilloscope for the simulation and practical testing of the amplifier to verify the performance of the designed High frequency Low noise amplifier. The design goals of noise figure of 0.52dB-0.7dB and bias conditions are Vcc = 3.5 V and Icc= 55 mA to produce 16.8 dB gain across the 0.4–2.2GHz band.

KEYWORDS

Amplifier, Bipolar Junction Transistor, Stability, LNA, Fabrication, Multism

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EXTENDED K-MAP FOR MINIMIZING MULTIPLE OUTPUT LOGIC CIRCUITS

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ABSTRACT

Minimization of multiple output functions of a digital logic circuit is a classic research problem. Minimal circuit is obtained by using multiple Karnaugh Maps (K-map), one for each function. In this paper we propose a novel technique that uses a single Karnaugh Map for minimizing multiple outputs of a single circuit. The algorithm basically accumulates multiple K-Maps into a single K-Map. Finding minimal numbers of minterms are easier using our proposed clustering technique. Experimental results show that minimization of digital circuits where more than one output functions are involved, our extended K-Map approach is more efficient as compare to multiple K-Map approach.

KEYWORDS

Boolean Algebra, Karnaugh Map, Digital Logic Circuit, Clustering

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